Energy Equip. Sys./ Vol. 5/No.2/ June 2017/197-210

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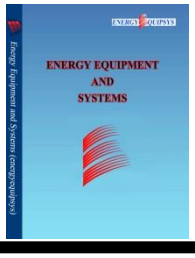

Distance protection closed-loop testing using RTDS

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Article history:

Received : 26 November 2016
Accepted : 11 January 2017

ABSTRACT

This paper presents a distance protection test procedure by applying the Real-Time Digital Simulator (RTDS) of a power system. RTDS is a tool to design, develop, and test power-system protection. The RTDS enables real-time computation of electromagnetic phenomena with a calculation time step of even 50μs. The hardware allows the import and export of many signals from the simulator to an external real power-system component and, therefore, the so-called closed-loop testing. With this method, it is possible to get an insight into both the elements' behaviour and the influence of these components on the power-system operation. The testing of a very simple impedance-protection function by the Schweitzer Engineering Laboratories protection relay is explained. Moreover, the effects of a DC offset have been tested on this relay. The test results emphasize the advantage of the RTDS for the determination of actual power-system components' behaviour in various power-system conditions. The RTDS software, i.e. RSCAD, is used to simulate the power system models.

Keywords: Distance Protection, DC Offset, Real-Time Electromagnetic Phenomena Calculation, RTDS.

1. Introduction

Novel software tools play an important role in the simulation and analysis of electrical power systems today. The software simulation of protective relays and power systems provides an acceptable method for inquiring and investigating the performance of protective relays in various situations.

Power-system producers have to thoroughly test their equipment before these are put into operation. Many tools are available for such test and, consequently, various approaches exist.

Based on the manuals of the available digital relays, precise digital relay models can be designed using programming language or advanced software like EMTP, PSCAD/EMTDC, and MATLAB Simulink [1–3]. Reference [4] presents an approach to test and validate several power-system dynamic-state-estimation algorithms using a Real Time Digital Simulator (RTDS), which, as the name suggests, is a real-time simulation tool. Moreover, Ananthan et al. [5] proposed a real-time hybrid model, which incorporates the advantages of both physical and numerical models with RTDS and Lab-VIEW. Reference [6] proposed a two-terminal travelling-wave-based fault-location algorithm. The fault locator routines were implemented using RTDS. In [7], a line-protection criterion is formed according to the phase difference between the voltage at the fault point and the compensatory voltage in the in-zone and out-of-zone faults.

This paper presents the RTDS along with its actual use in protection-relay closed-loop testing before the protection equipment is implemented in the power system. Such a simulator is widely accepted worldwide as a necessary tool to test power system control equipment in actual circumstances. In a real power system, such a test cannot be conducted. The achievable calculation time

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step is about 50μs and, if needed, it can be lowered to 1.5μs (for example, in FACTS devices' modelling) [8]. For this study, a test was conducted with a simple distance-protection scheme implemented into the protection relay of the Schweitzer Engineering Laboratories (SEL). The advantages of testing the equipment with an RTDS simulator are the conditions that can be simulated with RTDS. Moreover, relevant phenomena, such as harmonic distortion and frequency deviation, are included in the faults simulated in the RTDS model. As it turned out during relay testing, extra equipment had to be used with the RTDS simulator in most of the cases to convert and amplify the voltage signals produced by the simulator.

2. RTDS

RTDS is a real-time digital power-system simulator. It is unique in the sense that it works on the parallel processing technique of digital signal processors, executes the program developed on its processors, and produces output both graphically and through the output interface cards incorporated into the system. Power-system programs are developed using the RSCAD user interface, which is specially designed for RTDS and used to both develop different power system scenarios and view and study the results graphically [9]. The RTDS present in the research lab at Texas Tech University (TTU) consists of two racks with eight triple-processor cards and two Giga-processor cards. It also contains several input and output interface cards for sending and receiving analogue and digital signals. One of the important interface cards used in this study is the Digital-to-Analogue Converter Card (DACC) by which 12 signals can be sent out of the RTDS. In addition, the front-panel inputs are used to send digital control signals into the RTDS to control the elements in the simulated power system. Figure 1 show the RTDS front and back panels at TTU.

Detailed protective relay models can be created from RSCAD components and subjected to many test-case scenarios before the final implementation on the relay development platform. Model concepts and features can be subjected to the same test environment before and after the relay algorithm coding has been done.

The selected protection function is an impedance relay that provides basic protection for phase and ground faults. It uses a mho characteristic, polarized with positive-sequence memory voltage [10].

A four-shot auto-recloser logic scheme is presented as well. The calculation of impedance is simple in the RTDS, using the existing control components. Phase-to-phase and phase-to-ground impedances can be calculated using the three phase voltages and current quantities. Figure 2 demonstrates the block diagram of the software modules of RTDS.

Fig. 1. RTDS front and back panels

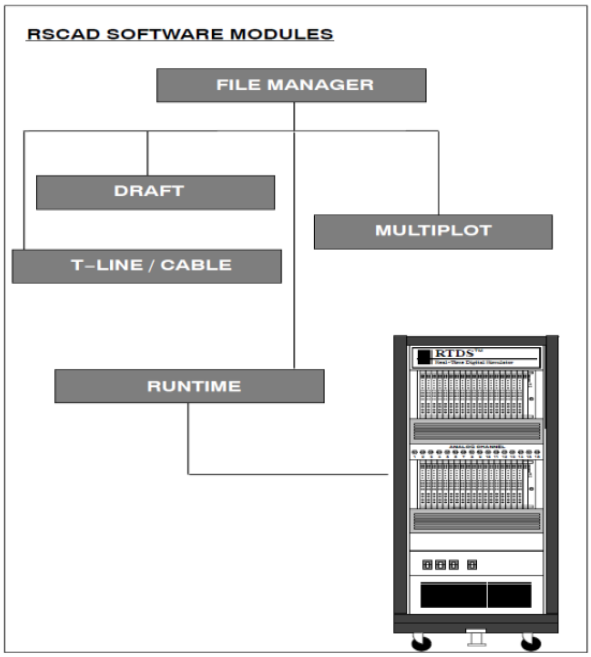

Fig. 2. RSCAD software modules

The basic steps involved in calculating the impedances [11] are:

1. Analogue signal sampling
2. DFT extraction of the fundamental values
3. Creating phase-to-phase values
4. Creating the $K_0 \times 3I_0$ factor for phase-ground calculations
5. Calculating the phase-to-phase and phase-to-ground impedance magnitudes

The relay model will provide the following user settings:

Line parameter settings:

Line parameter settings (with default K_0 calculation)

$$K_0 = \frac{Z_0 - Z_1}{3 \times Z_1} \quad (1)$$

Impedance relay settings:

1. Relay reach
2. Characteristic shape (it can be set to provide a circular, lens, or tomato shape).
3. Current supervision settings (ph-ph, phase, and $3I_0$ settings)

Automatic reclosure settings:

1. Shot count (number of reclosure attempts)
2. Circuit breaker open interval times for each attempt
3. Reclose reset time
4. Circuit breaker close pulse

The system model will provide the following user controls [11]:

1. Circuit breaker control logic
2. Fault control selection (LL, LG, LLG, etc.)
3. Point-on-wave control (fault inception)
4. Fault point (internal, external, or reverse)

The system model will provide the following components:

1. Source located at each end of a line.
2. Circuit breaker located at each end of the protected line.
3. Current transformer
4. Capacitive voltage transformer.

The advantages are:

1. Complete interaction between relays and the simulated power system
2. Testing several devices (relays and/or controllers)
3. Providing relay coordination
4. Providing numerous scenarios/settings in practical time

Figure 3 presents the closed-loop protective relay testing.

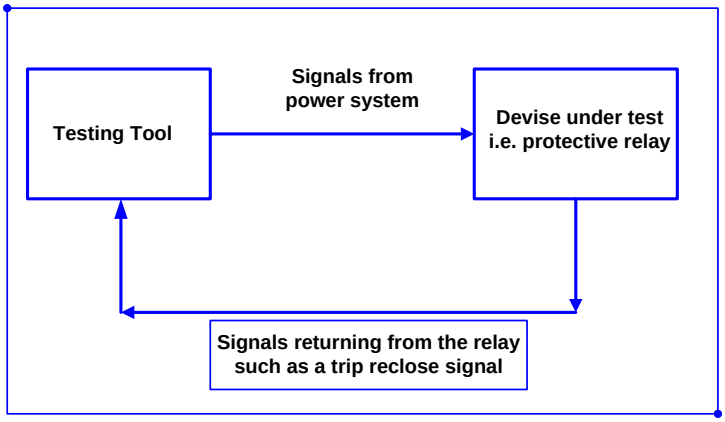

Fig. 3. The closed-loop protective relay testing

3. Distance relay

The multi-function distance relay is suitable for providing the distance-protection function on single-breaker transmission lines with single or three-pole tripping and reclosing schemes. An algorithm to detect secondary arc extinction is also available to help high-speed single-pole auto-reclosure schemes. Additional plot signals give enough information to help verify the theoretical calculations with simulation results.

3.1. Description

The distance-measuring zones include six impedance-measuring loops, three intended for phase-to-ground faults, and three for phase-to-phase faults.

The distance zones can have mho or quad characteristics. Additional impedance measurements can include the positive-, negative-, and zero-sequence components for plotting purposes. Phase selection and directional control are included, and so is the control logic for reclosure, communication-aided tripping, out-of-step detection, and breaker failure on open, closed, and secondary arc detection. The system frequency is determined using the instantaneous composite voltage: $V_a - 0.5V_b - 0.5V_c$.

If the system frequency changes, the sample rate also changes to ensure a constant eight samples per cycle. The measured system frequency and its rate of change can be monitored. The absolute difference between the composite voltage and the previous time-step composite voltage is used to detect disturbances in the voltage. If a disturbance is detected, frequency measurement and sample rate adjustment are suspended for three cycles.

3.2. Operation

The phase voltages and currents of distance relay are connected to the six inputs of the distance function. The positive-sequence memory voltage is created inside the relay, and an input is available for mutual coupling compensation as an import signal. The RMS values are calculated and the instantaneous impedance is measured for the phase-to-phase, phase-to-ground, positive, negative, and zero sequences. The distance elements are built using positive-sequence memory polarizing quantity when there is no reverse reach and the directly measured voltage when reverse reach is enabled. The distance elements are directly supervised by a directional element and a phase-selection element.

The distance-measuring zones for the phase-to-ground sequence will be compensated. This compensation factor can be calculated automatically following Eq.(1), or manually by entering the magnitude and angle values. The selected positive-, negative-, and zero-sequence voltages and currents used for the sequence-impedance calculations can be monitored in runtime or imported into the draft case as inputs to other control components.

4. Sel relay

The SEL-421 relay has a low-level test interface between the calibrated input module and the separately calibrated processing module. You can test the relay in either of these two ways: conventionally, by applying AC current signals to the relay inputs or by applying low-magnitude AC voltage signals to the low-level test interface. The low-level interface on the SEL relays will be used to connect to the RTDS. The RTDS will provide

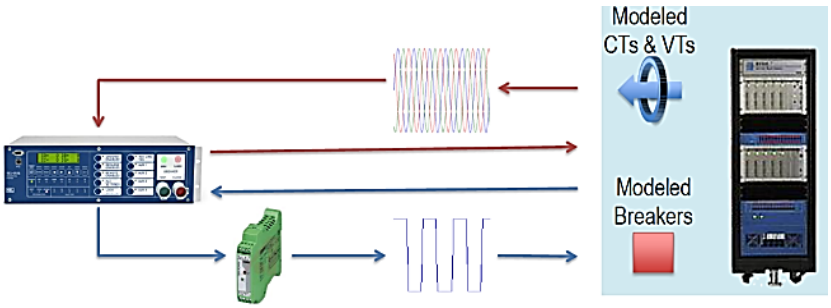

Fig. 4. SEL relay interfaced with RTDS [9]

represent the power-system voltages and currents. Figure 4 shows the SEL relay the necessary low-level AC signals that will interfaced with RTDS.

The component and component parameters' dialogue box are shown below. Figure 5 shows the DACC of relay and the number of outputs and inputs to the relay.

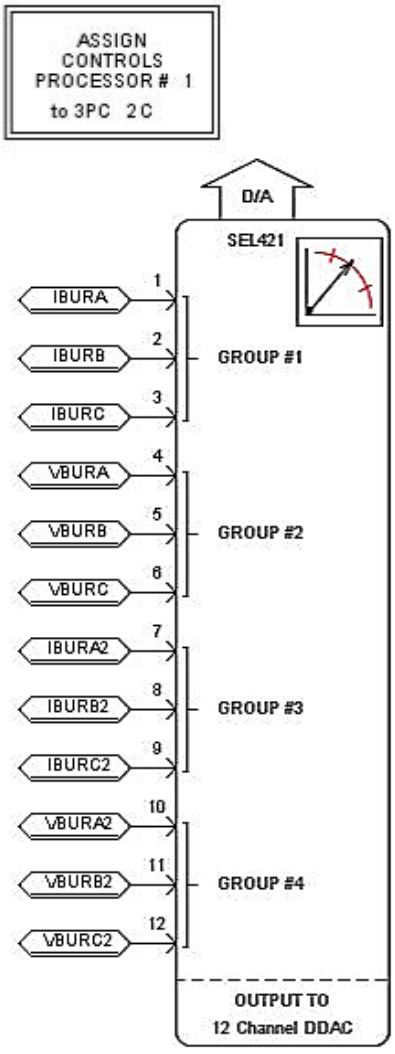

Fig. 5. Digital-to-analogue card of SEL relay [9]

The analogue output channel will be chosen so that the A-phase current is connected to channel 1, B phase is connected to channel 2, and C phase is connected to channel 3. The floating-point value is calculated using the scaling factor given by SEL for the appropriate relay being tested. We are given the low-level interface AC quantity that will produce nominal voltage or current when applied to the SEL relay. We also know that the RTDS analogue output channel needs a floating-point number 'SC' that will cause the RTDS to produce 5V when applied to the input [9]. In other words, we can easily calculate the floating-point number to enter into the 'SC' parameter by using the following formula [9]:

SEL-421 SC value for currents:

$$SC = \frac{5}{66.6 * 10^{-3}} * 5 = 375 \quad (2)$$

SEL-421 SC value for currents:

$$SC = \frac{5}{0.446} * 67 = 751 \quad (3)$$

The SEL-421 uses a 34-pin ribbon-cable female connector, which can be attached to one end of a ribbon cable, and the appropriate wire pairs can be connected to the RTDS DDAC analogue outputs. The 34-pin female connector is keyed and will only be inserted in one way. The multi-coloured ribbon cable contains sets of twisted pairs and will be used to connect from the SEL relay to the RTDS via the DB25 adapter on the front of the RTDS Portable.

The typical connection to SEL relay is shown in Fig. 6.

Fig. 6. Typical connections to SEL relay [9]

The SEL-421 binary output bits can be connected to the RTDS via the IEC61850-8-1 protocol.

5. Case study

5.1. System model

The modelling of the power system is done in RSCAD, the RTDS software.

The power system includes:

- A single transmission line consisting of a faulted line model
- A circuit breaker at each end of the transmission line
- A current transformer
- A capacitive coupled voltage transformer
- Fault switches to create internal faults, or forward-looking or reverse-looking faults.

5.2. Source model

A source model is often used to represent some portions of the power system in a simplified way. It generates a three-phase power - system frequency sine wave behind impedance. Since the internal magnitude, phase, and frequency do not change in response to changes in the system, the source model is sometimes referred to as an 'infinite source'.

5.3. Transmission line data

Transmission lines are generally modelled using travelling wave algorithms within the RTDS, based on data such as the line's modal impedances, travel times, and transformation matrix. A separate RSCAD software module called TLINE is available to generate these data from more commonly available line parameters. The total positive-sequence impedance of the protected line is 37.7Ω at 87.18°. The faulted-line model can be used to vary the fault location along the protected line. Forward faults are at 100% of the protected line length.

Reverse faults are at 20% of the protected line length behind the VTs and CTs.

Figure 7 shows the AC power system under study, and Fig. 8 demonstrates the RSCAD power system model with fault logic and relay logic.

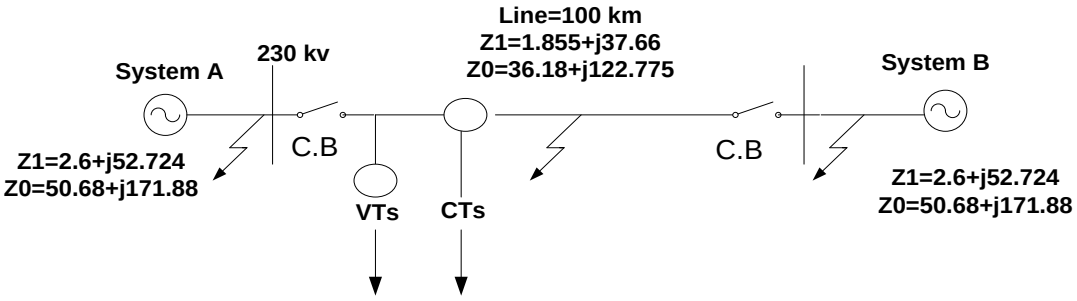

Fig. 7. Power system under test

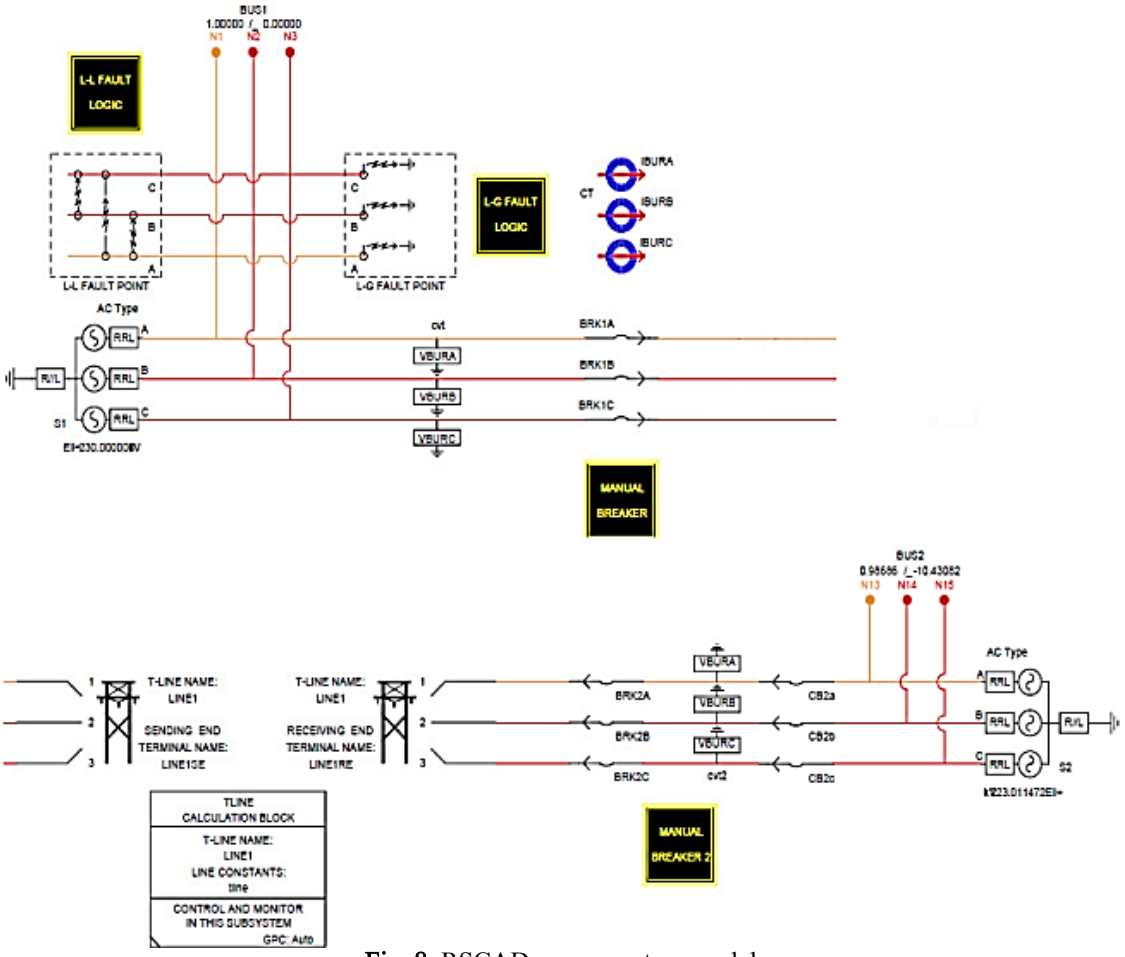

Fig. 8. RSCAD power system model

5.4. Fault branch

A fault branch may be connected to a bus to simulate a short circuit on that bus. The fault branch consists of a switch whose open resistance is very large and whose closed resistance is specified by the user.

The fault output is shown in Fig. 9.

5.5. Circuit breaker control

The circuit breaker (CB) logic is presented in Fig. 10. The CB operates in the same manner as the fault branch. A signal name is used to control the opening and closing of the circuit breaker contact.

The components used to create the CB-

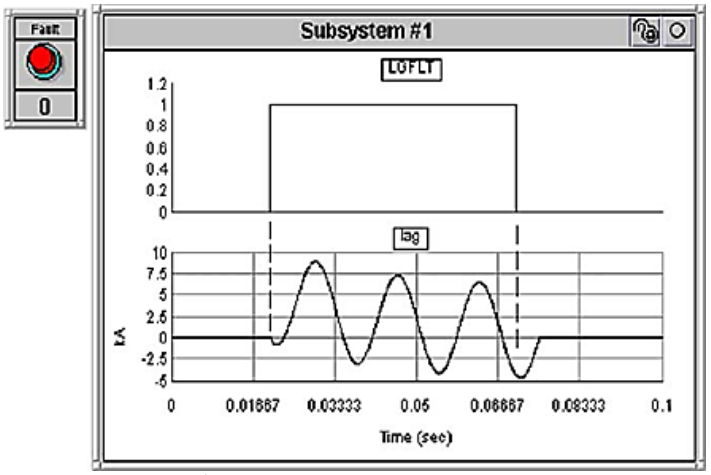

Fig. 9. The output of fault logic

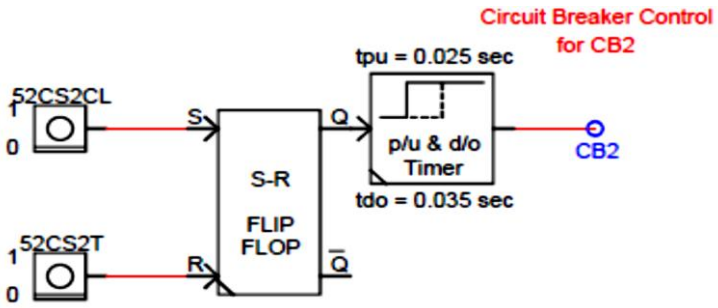

Fig. 10. CB logic

control signal name or words are as follows:

- Push button to open and close
- S-R flip-flop
- Pickup and dropout timer to simulate the operating time

6. Simulation results

6.1. Impedance calculation output

The used analogue signals involve three-phase voltage and three-phase current signals. The residual current is calculated within the algorithm and there will be no zero-sequence mutual coupling compensation.

The first decisions to be made are the type of sampling to be done, how often the input signal is sampled, and how the fundamental values are extracted from the sampled data. Most relay manufacturers sample the input signal at a much higher sample rate than the actual rate of the protection algorithm. Some algorithms operate at a slower or faster rate than the main protection algorithm. Relay algorithms that run at a different rate within the same relay are often referred to the rate of the processing thread within the processor running the algorithms.

For example, if a relay samples the input data at a rate of 96 samples per cycle, the analogue sampling is done in the 5760Hz (96*60) thread.

The protection algorithm for most relays operates at a much slower rate, usually only four to eight times per cycle. If the relay processes the protection algorithm at a rate of eight times per cycle, the algorithm operates in the 480Hz thread and the sampled data are needed eight times per cycle. The purpose of greater sample rates might be to provide a higher-quality recording of the transient conditions present in the input data during a system disturbance, assuming that a means has been provided for capturing the fault data and storing the data in records. The sampled data would normally be compressed before storage.

The circuit in the impedance calculation presented in Fig. 11 is discussed in five parts. The first part is used to sample the input. Phase voltage and phase current are measured at a point in the power system, which defines the impedance measurement origin. The phase voltage and phase current are sampled at 96 samples per cycle (5760Hz thread). The sampled data are then buffered into a moving average filter. The output of the moving average filter is sampled at eight samples per cycle (480Hz thread).

There is no anti-aliasing filtering on the input. Normally, a low-pass filter would be provided to prevent aliasing.

The purpose of the moving average filter is to reduce random noise (white noise) while still providing a sharp step response (12). The purpose of sampling the filtered data at eight samples per cycle is to provide a signal that is synchronous with the 480Hz thread in which the protection algorithm operates.

No frequency tracking is conducted to adjust the sample rate and to synchronize the protection algorithm with the system frequency. Most relay manufacturers will employ a method to ensure that the protection algorithm is synchronous with the system frequency. A Phase-Locked Loop (PLL) can be used to track the frequency to adjust the sampling rate. The PLL keeps the protection algorithm synchronous with the system frequency.

The second part of the impedance calculation circuit is incorporated to extract the fundamental values from the sampled input data. A full-cycle discrete Fourier transformer is used to create the real and imaginary values for the phasor

representation of values that are used to calculate the impedance magnitudes.

The third part of the impedance calculation circuit uses single-phase quantities to create the phase-to-phase values necessary for calculating the phase-to-phase impedance values.

The fourth part of the impedance calculation circuit uses the single-phase current quantities to create the zero-sequence current, which is then multiplied by the K0 factor, creating one of the necessary values used to calculate the phase-to-ground impedance [1]. Zero-sequence compensation is necessary to determine the correct magnitude of the phase-to-ground impedance for faults that include those in the ground. The value of compensation is determined using Eq.(1) and the values of the positive-sequence impedance (Z1) and zero-sequence impedance (Z0) are determined for the transmission line.

The fifth part of the impedance calculation circuit incorporates the magnitude quantities calculated in parts 3 and 4 to calculate the impedances for phase-to-phase and phase-to-ground magnitudes.

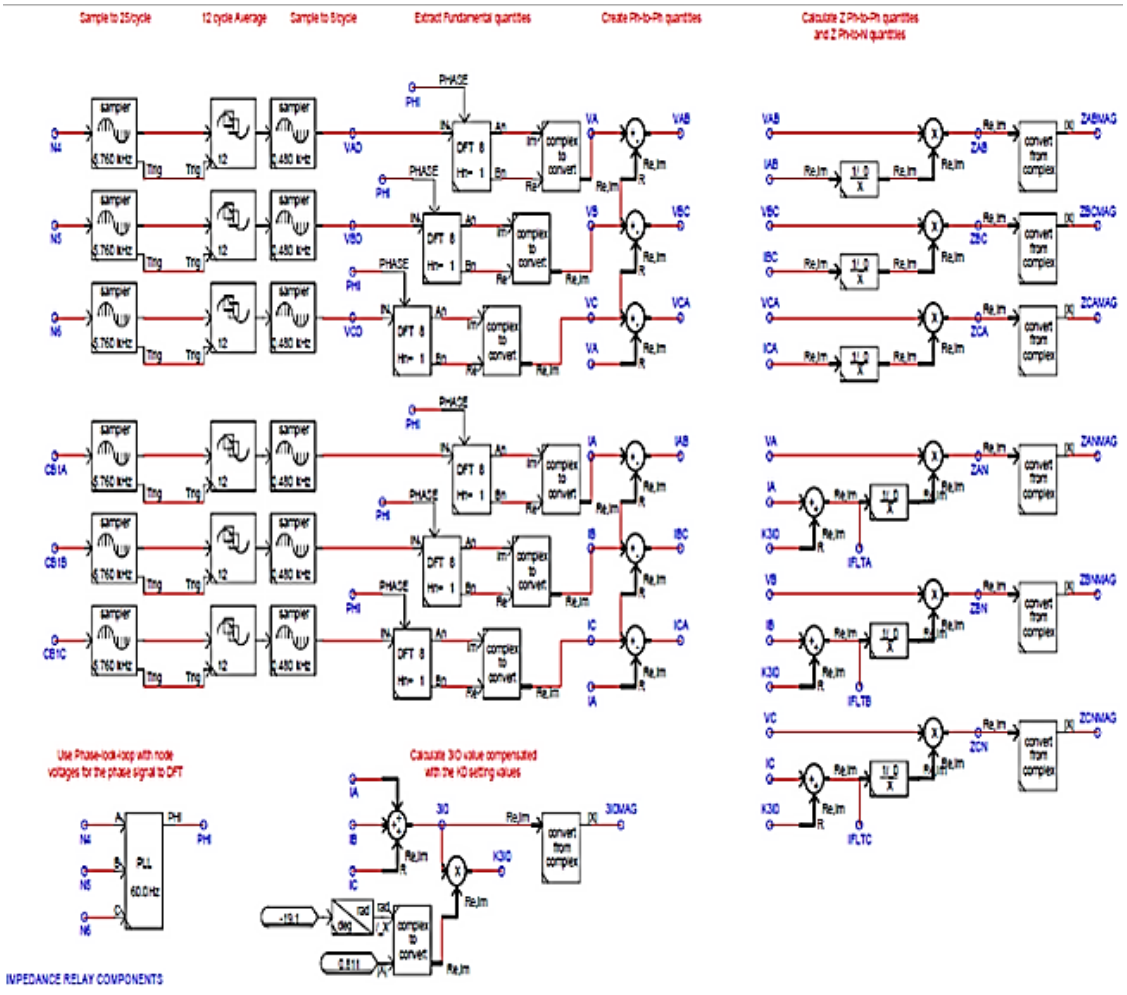

Fig. 11. Block diagram and logic of impedance calculation

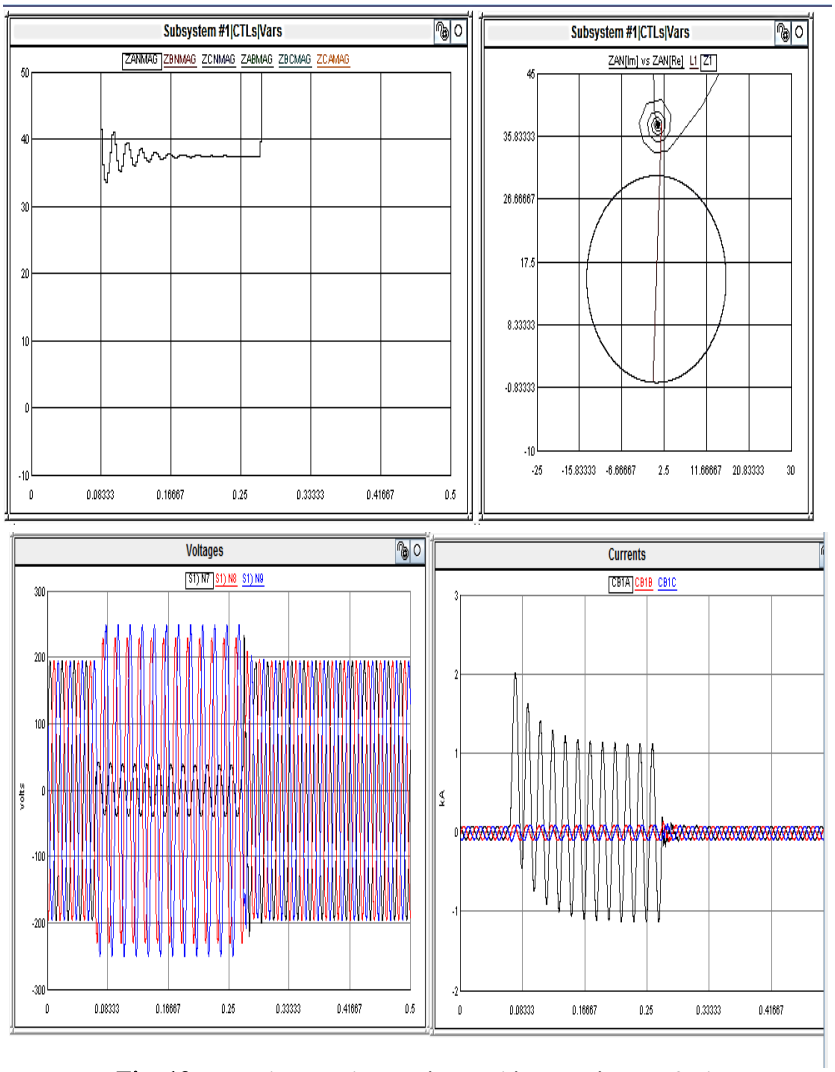

Fig. 12. Impedance relay testing and its reaction on fault

Using Fig. 11, the reaction of relay can be seen in Fig. 12. The latter shows the draft case from step 4, broken into discrete component blocks. As many hierarchal blocks as necessary can be made. Step 4 shows the hierarchal blocks grouped into control logic components, impedance relay components, and relay threshold components. The name of each hierarchal block has been chosen to represent the corresponding function contained within it.

6.2. DC offset effect on impedance

The effect of the DC offset component of distance relay in the fault current can be seen in Fig. 13. The RX plot of the A phase to neutral impedance with DC offset has been presented for a fault at the end of the protected line. The blue circle is the typical normal mho characteristic setting of 80% reach of positive-sequence impedance for the line. The black line shows the impedance trajectory during the fault and the effect of the decaying DC component included in the fault current. The overreach effect caused by the overestimation of the fundamental current magnitude due to the DFT calculation is observed as a circular rotation around the actual fault locus situated at the end of the line 'L1' along the positive sequence-line angle. The effect of this rotation around the fault locus will be further exaggerated by the effect of sub-harmonic oscillations in the fault voltage signal when a capacitive-coupled voltage transformer is used to provide the secondary voltages. The proper removal of this exponentially decaying DC component will help the distance functions [13] perform a more accurate calculation during faults.

The next step includes a DC-removal algorithm, which is implemented using the RSCAD Component Builder application. Figure 14 shows considerable improvement in

the performance of the impedance calculation compared with that of the same fault shown in Fig. 13.

The simple algorithm provides a useful example of how a DC-removal filter should perform. The algorithm provides almost full rejection of any decaying waveform that could be present in the signals provided by CTs and CVTs.

This approach is simple and independent of X/R ratios of the protected line. A decaying DC component can be removed without making too many calculations in the DSP.

The purpose of this example is to show

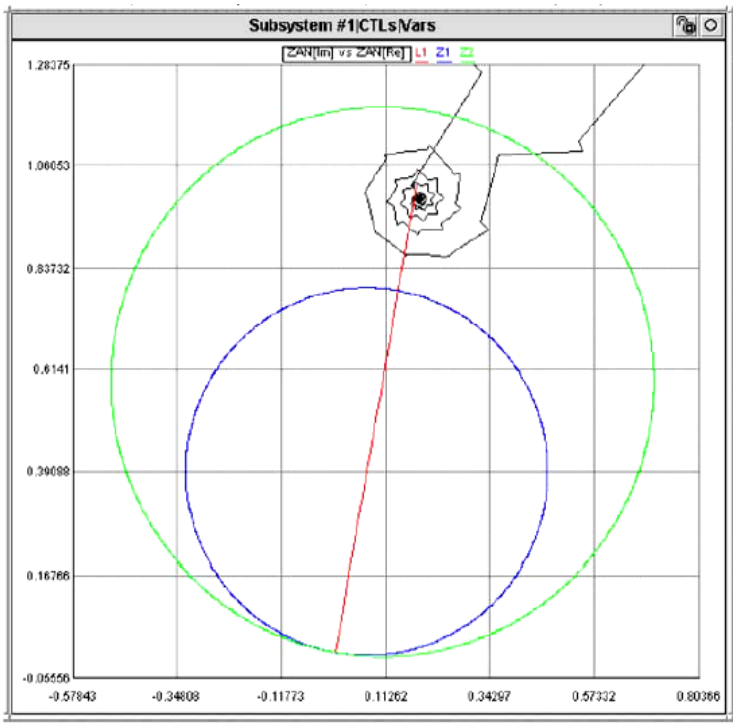

Fig. 13. RX plot of impedance with DC offset

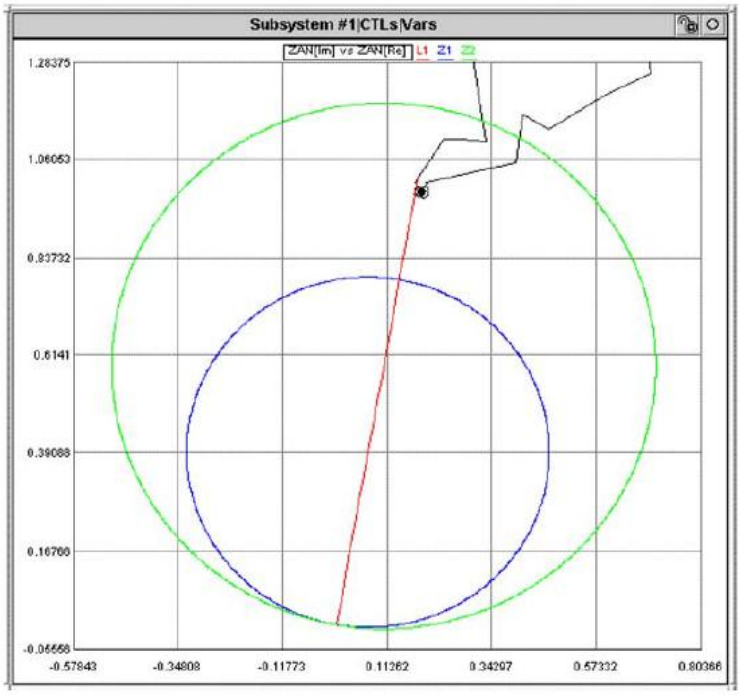

Fig. 14. RX plot of impedance A−N with DC offset removal

how a decaying DC component will have an adverse impact on impedance calculations. The algorithm assumes a synchronous sample rate with no substantial harmonic content in the input signal. The algorithm will make a gain of 1.0 at the fundamental frequency with 0.0° phase shift and 0.0 gains at DC. Consider three signals, equal in magnitude but separated by 45° in an input buffer; N0=1pu at 0°, N1=1pu at −45°, and N2=1pu at −90°. The two oldest signals are added to form a new signal called NS. The NS signal is subtracted from the previous new sample, which we name 'old sample' (OS). The NS subtracted from OS then provides the filter output called Y. The fact that Y is effectively differentiated provides us with a good DC-rejection characteristic. The phase error is also minimized, as it can be seen from the fact that Y lies along the same trajectory as N0.

The input data are sampled at 480Hz or eight samples per cycle. The sampled data are held in a three-state buffer. Sample 1 is represented by signal N0 at 0°, sample 2 by signal N1 at −45°, and sample 3 by signal N2 at −90°.

Figure 15 demonstrates the filtered output of the input waveform that consists of a 1-pu, 60-Hz sinusoid wave combined with a 0.25-pu, 6-Hz saw-tooth wave. The red waveforms represent the input signals and the blue waveforms represent the filtered waveforms. It can be observed that the algorithm almost completely removes the unwanted saw-tooth waveform and provides the desired sinusoid. The DC-removal filter in the RSCAD environment is shown in Fig 16. Also, Fig. 17 shows the phasor diagram of DC removal.

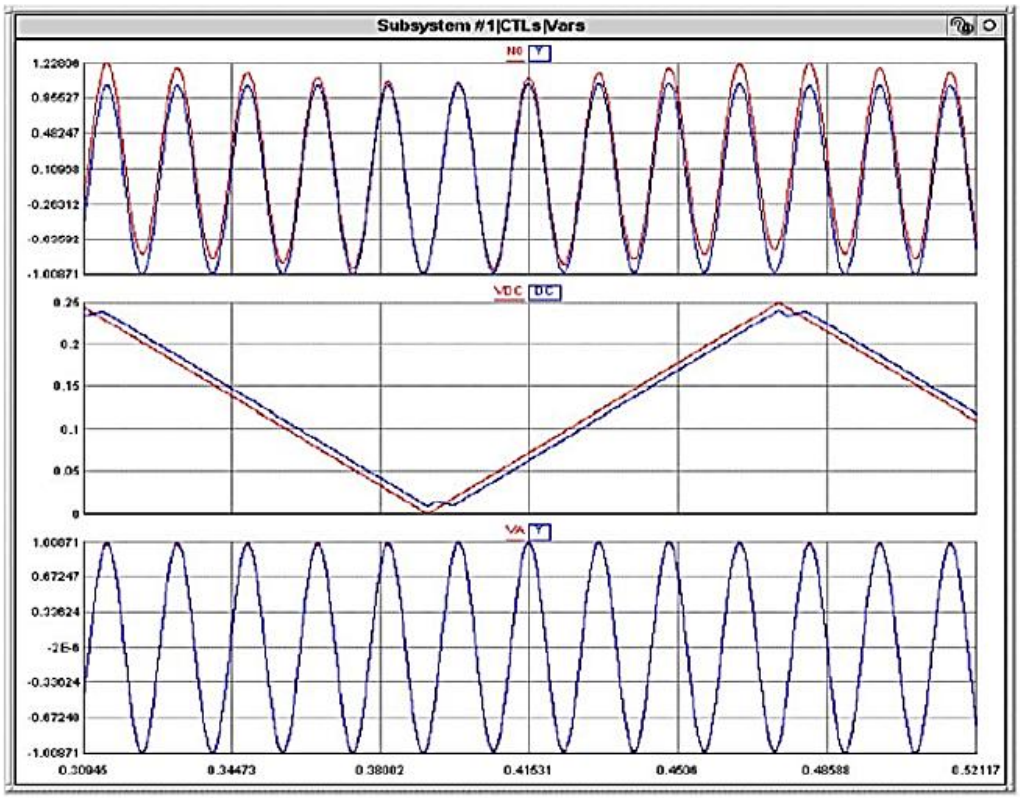

Fig. 15. DC-removal waveforms

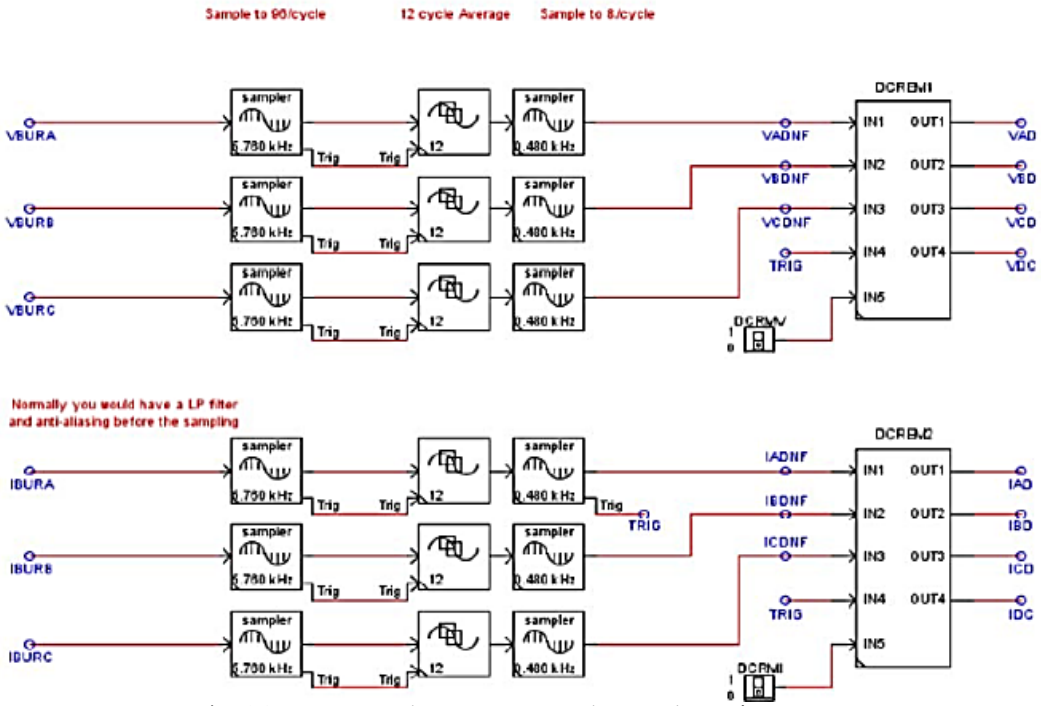

Fig. 16. DC-removal component used on analogue inputs

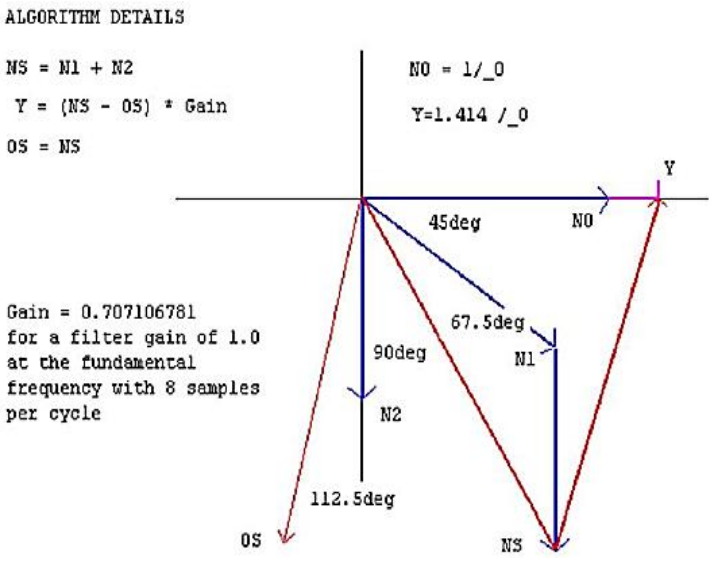

Fig. 17. Phasor diagram of DC removal

7. Conclusion

The main purpose of this paper was to present the power-system RTDS along with its actual use in the area of the protection relay closed-loop testing before the protection equipment is implemented in the power system. Such a simulator is widely accepted worldwide as a necessary tool to protect power systems and test control equipment in actual circumstances.

In a real power system, such tests cannot be done. The achievable calculation time step is about 50μs and, if needed, can be lowered to 1.5μs (for example, FACTS devices' modelling). For the purpose of this study, a test was conducted on a simple distance-protection scheme implemented by the SEL-protection relay. Moreover, relevant

phenomena, such as harmonic distortion and frequency deviation, were included in the faults simulated in the RTDS model. As it turned out during the relay testing, in most cases, extra amplifying equipment had to be used besides the RTDS simulator to convert and amplify the voltage signals produced by the simulator.

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